In the Claims:

Claims 1-4 (Canceled).

Claim 5 (Currently amended): A method of manufacturing a semiconductor memory device, comprising the steps of:

a) forming gate electrodes on a substrate having a cell region and a periphery region;

b) forming a first insulating layer over the substrate, the first insulating layer covering the gate electrodes;

c) forming first metal contact holes and stud holes in the first insulating layer, wherein the stud holes are aligned with corresponding one of the first metal contact holes;

d) forming metal contact studs and first metal contact portions in the stud holes and the first metal contact holes, respectively;

e) forming a second insulating layer on the first insulating layer and on the metal contact studs;

f) forming bit line contact holes passing through the first and second insulating layers;

g) forming bit line contacts in the bit line contact holes; and

h) forming bit lines on the second insulating layer, wherein the metal contact studs are formed having a width that is greater than a space between adjacent bit lines.

Claim 6 (Original): The method of claim 5, further comprising the steps of:

i) forming a capacitor over the cell region of the substrate;

j) forming a third insulating layer over the substrate, said third insulating layer covering the bit lines;

k) forming second metal contact holes in the second and third insulating layers, the second metal contact holes exposing a portion of the metal contact studs; and

l) forming second metal contacts in the second metal contact holes.

Claim 7 (Currently amended): The method of claim 5, wherein the step of forming the stud holes further comprises the steps of:

forming a first photoresist pattern on the first insulating layer;

isotropically and partially etching the first insulating layer using the first photoresist pattern as an etching mask to form the stud holes;

anisotropically etching the first insulating layer using the first photoresist pattern as an etching mask to form the first metal contact holes which are narrower than the stud holes; and

removing the first photoresist pattern.

~~etching the stud holes in the first insulating layer using the first photoresist pattern as a mask, wherein after the stud holes are formed, the first photoresist pattern is removed.~~

Claim 8 (Original): The method of claim 5, wherein the first metal contact holes are formed using anisotropic etching processing to expose a portion of an active area and at least one of said gate electrodes.

Claim 9 (Original): The method of claim 5, wherein the step of (d) further comprises the steps of:

depositing a first conductive material layer on the first insulating layer, wherein said first conductive material layer fills the stud holes and the first metal contact holes; and

removing a portion of the first conductive material layer to form the metal contact studs and the first metal contact portions.

Claim 10 (Original): The method of claim 5, wherein the step of (e) further comprises the step of planarizing the second insulating layer using a chemical mechanical polishing (CMP) technique.

Claim 11 (Original): The method of claim 5, wherein the step of (f) further comprises the steps of:

forming a second photoresist pattern on the second insulating layer; and

etching the first and second insulating layers to form the bit line contact holes using the second photoresist pattern as a mask, wherein after the bit line contact holes are formed, the second photoresist pattern is removed.

Claim 12 (Original): The method of claim 5, wherein the step of (g) further comprises the steps of:

depositing a second conductive material layer on the second insulating layer, the second conductive material layer filling the bit line contact holes; and

removing a portion of the second conductive material layer on the second insulating layer.

Claim 13 (Original): The method of claim 5, wherein step (h) further comprises the steps of:

depositing a third conductive material layer on the second insulating layer, wherein the third conductive material layer contact the bit line contacts; and

patterning the third conductive material layer to form the bit lines.

Claim 14 (Original): The method of claim 5, wherein an area of a lower portion of each metal contact stud is less than an area of an upper portion of each metal contact stud.

Claim 15 (Currently amended): The method of claim 6, wherein step (k) further comprises the steps of:

forming third photoresist patterns on the third insulating layer;

etching the third insulating layer and the second insulating layer using the third photoresist patterns as a mask to form the second metal contact holes, wherein each of the second metal contact holes pass through between the adjacent bit lines and exposes a portion of the metal contact studs.

Claim 16 (Original): The method of claim 6, wherein step (l) further comprises the steps of:

depositing a fourth conductive material layer on the third insulating layer, the fourth conductive material layer filling the second metal contact holes; and

removing a portion of the fourth conductive material layer on the third insulating layer to form the second metal contacts.

Claim 17 (Original): The method of claim 12, wherein at least one of the bit line contacts is connected to active area of the substrate.

Claim 18 (Original): The method of claim 12, wherein at least one of the bit line contacts is connected to one of the gate electrodes.

Claim 19 (New): A method of manufacturing a semiconductor memory device, comprising the steps of:

forming lower portions of metal contacts and metal studs in a first insulating layer disposed on a substrate having gate electrodes, wherein each of the metal studs is aligned with corresponding one of the lower portions of the metal contacts;

forming a second insulating layer on the first insulating layer and on the metal studs;

forming bit line contacts that pass through the first and the second insulating layers;

forming bit lines on the second insulating layer and in contact with the bit line contacts;

forming a third insulating layer on the second insulating layer and the bit lines; and

forming upper portions of the metal contacts that pass through the second and the third insulating layers, wherein each of the upper portions of the metal contacts is in contact with one of the metal studs and is disposed between adjacent bit lines, and wherein each of the metal contact studs is formed having a width that is greater than a space between adjacent bit lines.

Claim 20 (New): The method of claim 19, wherein the step of forming lower portions of metal contacts and metal studs in a first insulating layer:

forming a first photoresist pattern on the first insulating layer; and

etching stud holes in the first insulating layer using the first photoresist pattern as a mask.

Claim 21 (New): The method of claim 20, further comprising steps of:

forming lower contact holes for the lower portions of the metal contacts using anisotropic etching process within an area of the stud holes such that a width of the lower contact holes is narrower than a width of the stud holes.

Claim 22 (New): The method of claim 21, wherein the anisotropic etching process exposes a portion of an active area and at least one of said gate electrodes, and wherein after the lower contact holes for the lower portions of the metal contacts are formed, the first photoresist pattern is removed.

Claim 23 (New): The method of claim 22, further comprising the steps of:

depositing a conductive material layer on the first insulating layer, wherein the conductive material layer fills the stud holes and the lower contact holes; and

removing a portion of the conductive material layer to form the metal contact studs and the lower portions of the metal contacts such that a surface of the first insulating layer and a surface of the metal contact studs are exposed, wherein the surface of the first metal contact studs is substantially co-planner with the surface of the first insulation layer.

Claim 24 (New): The method of claim 19, wherein forming the upper portions of the metal contacts further comprises the steps of:

forming third photoresist patterns on the third insulating layer;

etching the third insulating layer and the second insulating layer using the third photoresist patterns as a mask to form upper contact holes for the upper portions of the metal contact holes, wherein each of the upper contact holes is disposed between the adjacent bit lines and exposes a portion of one of the metal contact studs;

depositing a conductive layer on the third insulating layer, the conductive layer filling the upper contact holes; and

removing a portion of the conductive layer on the third insulating layer to form the upper portions of the metal contacts.